

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (Currently amended) A method for latching and amplifying a
2 capacitively coupled inter-chip communication signal, comprising:
3 receiving an input signal on a capacitive receiver pad from a capacitive
4 transmitter pad;
5 feeding the input signal through an inverter to produce an output signal;
6 feeding the output signal through a weakened inverter to produce a
7 feedback signal;
8 adjusting an RC time constant for the feedback signal so that the time
9 constant for the feedback signal is significantly larger than the time constant for
10 the transmitted signal from the capacitive transmitter pad, thereby ensuring that
11 the feedback signal does not mask transitions of the transmitted signal;
12 feeding the feedback signal back into an input of the inverter so as to form
13 a latch for the input signal between the inverter and the weakened inverter; and
14 establishing a high bias voltage, V_H , with a high bias voltage generator and
15 establishing a low bias voltage, V_L , with a low bias voltage generator;
16 wherein the high bias voltage generator includes a mechanism for
17 adjusting the high bias voltage, V_H ;
18 wherein the low bias voltage generator includes a mechanism for adjusting
19 the low bias voltage, V_L ;
20 wherein the weakened inverter is biased to produce the feedback signal
21 that swings between the high bias voltage, V_H , and the low bias voltage, V_L ; and

22 wherein V_H is slightly higher than a switching threshold of the inverter, and
23 V_L is slightly lower than the switching threshold of the inverter, whereby the
24 feedback signal causes the input signal to reside within a narrow voltage range
25 near the switching threshold of the inverter, thereby making the inverter sensitive
26 to small transitions in the input signal received on the capacitive receiver pad.

1 2. (Original) The method of claim 1, further comprising amplifying an
2 output of the inverter through an amplification stage to produce an amplified
3 output signal.

1 3-4 (Canceled).

1 5. (Previously presented) The method of claim 2, further comprising
2 adjusting the high bias voltage generator and the low bias voltage generator to
3 provide a specified sensitivity to transitions of the input signal.

1 6. (Previously presented) The method of claim 2, further comprising
2 adjusting the high bias voltage generator and the low bias voltage generator to
3 provide a specified noise immunity to noise associated with the input signal.

1 7 (Canceled).

1 8. (Currently amended) An apparatus for latching and amplifying a
2 capacitively coupled inter-chip communication signal, comprising:
3 a receiving mechanism configured to receive an input signal on a
4 capacitive receiver pad from a capacitive transmitter pad;
5 a latching mechanism configured to feed the input signal through an
6 inverter to produce an output signal; and

7 a biasing mechanism configured to establishing a high bias voltage, V_H ,
8 with a high bias voltage generator and establishing a low bias voltage, V_L , with a
9 low bias voltage generator; and
10 an adjusting mechanism configured to adjust an RC time constant for the
11 feedback signal so that the time constant for the feedback signal is significantly
12 larger than the time constant for the transmitted signal from the capacitive
13 transmitter pad, thereby ensuring that the feedback signal does not mask
14 transitions of the transmitted signal;
15 wherein the high bias voltage generator includes a mechanism for
16 adjusting the high bias voltage, V_H ;
17 wherein the low bias voltage generator includes a mechanism for the low
18 bias voltage, V_L ;
19 wherein the latching mechanism is further configured to feed the output
20 signal through a weakened inverter to produce a feedback signal;
21 wherein the latching mechanism is further configured to feed the feedback
22 signal back into an input of the inverter so as to form a latch for the input signal
23 between the inverter and the weakened inverter;
24 wherein the weakened inverter is biased to produce the feedback signal
25 that swings between the high bias voltage, V_H , and the low bias voltage, V_L ; and
26 wherein V_H is slightly higher than a switching threshold of the inverter, and
27 V_L is slightly lower than the switching threshold of the inverter, whereby the
28 feedback signal causes the input signal to reside within a narrow voltage range
29 near the switching threshold of the inverter, thereby making the inverter sensitive
30 to small transitions in the input signal received on the capacitive receiver pad.

1 9. (Original) The apparatus of claim 8, further comprising an amplifying
2 mechanism configured to amplify an output of the inverter through an
3 amplification stage to produce an amplified output signal.

1 10-11 (Canceled).

1 12. (Previously presented) The apparatus of claim 9, further comprising an
2 adjusting mechanism configured to adjust the high bias voltage generator and the
3 low bias voltage generator to provide a specified sensitivity to transitions of the
4 input signal.

1 13. (Previously presented) The apparatus of claim 9, further comprising an
2 adjusting mechanism configured to adjust the high bias voltage generator and the
3 low bias voltage generator to provide a specified noise immunity to noise
4 associated with the input signal.

1 14 (Canceled).

1 15. (Currently amended) A means for latching and amplifying a
2 capacitively coupled inter-chip communication signal, comprising:
3 a receiving means for receiving an input signal on a capacitive receiver
4 pad from a capacitive transmitter pad;
5 a latching means configured to feed the input signal through an inverter to
6 produce an output signal; and
7 a biasing means for establishing a high bias voltage, V_H , with a high bias
8 voltage generator and for establishing a low bias voltage, V_L , with a low bias
9 voltage generator;
10 an adjusting means for adjusting an RC time constant for the feedback
11 signal so that the time constant for the feedback signal is significantly larger than
12 the time constant for the transmitted signal from the capacitive transmitter pad,
13 thereby ensuring that the feedback signal does not mask transitions of the
14 transmitted signal;

15 wherein the high bias voltage generator includes a mechanism for
16 adjusting the high bias voltage, V_H ; and
17 wherein the low bias voltage generator includes a mechanism for the low
18 bias voltage, V_L ;
19 wherein the latching means is further configured to feed the output signal
20 through a weakened inverter to produce a feedback signal;
21 wherein the latching means is further configured to feed the feedback
22 signal back into an input of the inverter so as to form a latch for the input signal
23 between the inverter and the weakened inverter;
24 wherein the weakened inverter is biased to produce the feedback signal
25 that swings between the high bias voltage, V_H , and the low bias voltage, V_L ; and
26 wherein V_H is slightly higher than a switching threshold of the inverter, and
27 V_L is slightly lower than the switching threshold of the inverter, whereby the
28 feedback signal causes the input signal to reside within a narrow voltage range
29 near the switching threshold of the inverter, thereby making the inverter sensitive
30 to small transitions in the input signal received on the capacitive receiver pad.

1 16. (Original) The means of claim 15, further comprising an amplifying
2 means for amplifying an output of the inverter through an amplification stage to
3 produce an amplified output signal.

1 17-18 (Canceled).

1 19. (Previously presented) The means of claim 16, further comprising an
2 adjusting means for adjusting the high bias voltage generator and the low bias
3 voltage generator to provide a specified sensitivity to transitions of the input
4 signal.

1 20. (Previously presented) The means of claim 16, further comprising an
2 adjusting means for adjusting the high bias voltage generator and the low bias
3 voltage generator to provide a specified noise immunity to noise associated with
4 the input signal.

1 21-24 (Canceled).